As to (a)(2), the claims from the above-noted patent which applicant herein believes interfere are numbered 1, 2, 4 to 7, 9, 11 and 12. Claims 1, 9 and 12 of these claims are proposed counts in the requested interference. These proposed counts correspond to the listed claims since they are identical thereto.

As to (a)(3), claims 1, 9 and 12 of Nowak et al. are identical to claims 21, 27 and 29 respectively of the subject application, this providing the required correspondence.

As to (a)(4), applicant will prevail because the subject matter of the subject application is completely contained in provisional application number 60/026,769, filed September 26, 1996, from which priority has been claimed, whereas Nowak et al. bears a filing date of February 20, 1997.

As to (a)(5), support for claims 21 to 29 in the subject application is set forth as follows:

21. A dynamic logic circuit, comprising:

a precharge transistor (3) connected to a power source for precharging a node (A) for indicating a first logic level upon receiving a precharge signal (page 6, lines 13ff (Fig. 1), page 7, lines 4 to 6, (Fig. 3));

discharge means (5, 11, page 6, lines 20 to 24, (Fig. 1)) for discharging said node to indicate a second logic level; and

a switch (15, page 7, lines 1 to 10, (Fig. 3)) for connecting said precharge signal to said precharge transistor, said

switch connected to pass said precharge signal to said precharge transistor if said node has been previously discharged to said second logic state.

22. A dynamic logic circuit as recited in claim 21, further comprising:

a keeper transistor (17, page 7, lines 10 to 21, (Fig. 3)) connected between said power source and a gate of said precharge transistor for keeping said node at said first logic level prior to discharging with said discharging means.

23. A dynamic logic circuit as recited in claim 22 wherein a gate of said keeper transistor is connected to an output of said dynamic logic circuit (17, page 7, lines 10 to 21, (Fig. 3)).

24. A dynamic logic circuit as recited in claim 22, further comprising a half keeper latch comprising a transistor (19, page 7, lines 10 to 21, (Fig. 3)) connected between said power source and said node and having a gate connected to an output of said dynamic logic circuit.

25. A dynamic logic circuit as recited in claim 23, further comprising a full keeper latch comprising:

a first transistor (19, page 7, lines 10 to 21, (Fig. 3)) connected between said power source and said node and having a gate connected to an output of said dynamic logic circuit; and

a second transistor connected between said node and electrical ground, and having a gate connected to said output of said dynamic logic circuit (11, the gate of which is connected to the circuit output via a transistor 3 or transistor 17 (Fig. 3)).

26. A dynamic logic circuit as recited in claim 21 wherein said discharge means comprises a series of transistors for realizing a logical AND function (page 6, lines 5 to 6, transistors 5 and 11 can and do provide an AND function when used for such purpose).

27. A precharge circuit for a dynamic CMOS circuit (while CMOS is not expressly stated, the circuitry depicted is obviously CMOS), comprising:

a precharge node (A, page 6, lines 2 to 24, (Fig. 1)) for holding a first voltage level indicating a first logic state ;

a precharge transistor (3, page 6, lines 13ff, (Fig. 1)) connected between said precharge node and a voltage source;

a keeper transistor (17, page 7, lines 10 to 21, (Fig. 3)) connected between a gate of said precharge transistor and said voltage source for keeping said precharge node at said first voltage level indicating said first logic state prior to discharge; and

a switching transistor (15, page 7, lines 1 to 10, (Fig. 3)) controlled by a feedback signal indicating a logic state of said precharge node; said switching transistor activating said precharge transistor during a stand-by cycle only if said precharge node has been previously discharged to a second level indicating a second logic state.

28. A precharge circuit for a dynamic CMOS (while CMOS is not expressly stated, the circuitry depicted is obviously CMOS) circuit as recited in claim 27 wherein a gate of said keeper transistor is connected to an output of said dynamic logic circuit (17, page 7, lines 10 to 21, (Fig. 3)).

29. A method of precharging a dynamic CMOS (while CMOS is not expressly stated, the circuitry depicted is obviously CMOS) circuit, comprising the steps of:

precharging a node (A, page 6, lines 2 to 24, (Fig.1)) to a high voltage level indicating a first logic state during a stand-by mode;

discharging said node with connected logic circuitry (5 to 11, page 6, lines 2 to 12) if said logic circuitry is activated during an active mode;

precharging said node during a subsequent stand-by mode if said node was discharged during said discharging step (15, page 7, lines 1 to 21); and

inhibiting the precharging of said node during said subsequent stand-by mode if said node remains precharged from a previous standby (feedback from output to 15, page 7, lines 1 to 21).

As to (a)(6), the constructive reduction to practice is based upon provisional application 60/026,769, the specification of which, on information and belief, is identical to that of the subject application and the claims are therefore readable thereon as noted above with reference to the subject application,

As to (d), applicant will be senior party on the present record and need supply nothing further at this time. Applicant does, however, reserve his right to show earlier activity than that set forth in the provisional application, should that be necessary.

In view of the above remarks, it is respectfully requested that the interference declared with Tran being declared senior party.

Respectfully submitted,

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